Amendments to the Specification

Please replace the title with the following amended title:

SEMICONDUCTOR DEVICE INCLUDING PLURAL CHIPS WITH PROTRUDING EDGES LAMINATED ON A DIE PAD SECTION ~~AND MANUFACTURING METHOD THEREOF~~

Please replace the paragraph beginning on page 5, line 9 with the following amended paragraph:

~~Fig. 7 shows~~ Figs. 7(a) and 7(b) show physical-property values of respective parts of the simulation model;

Please replace the paragraph beginning on page 5, line 12 with the following amended paragraph:

~~Fig. 9 shows~~ Figs. 9(a) and 9(b) show level-by-level averages of maximum stresses over the entire semiconductor device;

Please replace the paragraph beginning on page 5, line 14 with the following amended paragraph:

~~Fig. 10 depicts~~ Figs. 10(a) and 10(b) depict level-by-level averages of maximum stresses at an edge portion;

Please replace the paragraph beginning on page 5, line 19 with the following amended paragraph:

~~Fig. 12 is a~~ Figs. 12(a) and 12(b) are cross-sectional [[view]] views of a semiconductor device 1 according to a second embodiment of the present invention;

Please replace the paragraph beginning on page 5, line 24 with the following amended paragraph:

~~Fig. 14 illustrates~~ Figs. 14(a) and 14(d) illustrate examples of shapes of through portions;

Please replace the paragraph beginning on page 15, line 9 with the following amended paragraph:

~~Fig. 7 shows~~ Figs. 7(a) and 7(b) show respective parts of the simulation model. Fig. 7(a) illustrates elastic moduli and Poisson's ratios of a base material for the semiconductor chips 4 and 5, the lead frame 2, the resin encapsulating body 10 and the adhesives 6 and 7. As shown in Fig . 7(a), the resin encapsulating body 10 is small in elastic modulus and large in Poisson's ratio as compared with the base material for the semiconductor chips 4 and 5 and the lead frame 2. The difference between the elastic modulus and the Poisson's ratio referred to above leads to the occurrence of large stress in the lead frame 2 and the semiconductor chips 4 and 5. Fig . 7(b) shows conditions (dimensions) used in simulation for every amount of displacement A, chip

thickness B and the half C of die pad length. Here, the respective dimensions are represented in the form of ratios set with a half X = 5.7mm of the distance between the sides 53 and 54 of the semiconductor chip 5 as the reference. For instance, when the condition is 1 = 0.1, the amount of displacement A is represented as 0.1 X 5.7 = 0.57mm. When the condition is 1 = 0.02, B is represented as 0.02 x 5.7= 0.114mm. When the condition is that the chip thickness is 1 – 0.7, the half C of die pad length is represented as 0.7 X 5.7 = 3.99mm.

Please replace the paragraph beginning on page 17, line 13 with the following amended paragraph:

It is understood that at the mention of the amount of displacement A by referring to ~~Figs. 9 and 10~~ Figs. 9(a) and 9(b) and Figs. 10(a) and 10(b), the stress applied onto the entire semiconductor device 1 does not show a noticeable change according to the amount of displacement A, whereas the stress at the edge portion E becomes gradually large with an increase in the amount of displacement A. As to the chip thickness B, the stress applied onto the entire semiconductor device 1 decreases with an increase in the chip thickness B, whereas the stress at the edge portion E increases from the chip thickness B1 to the chip thickness B2 and decreases from the chip thickness B2 to the chip thickness B3. It is understood that as to the half C of die pad length, the stress applied onto the entire semiconductor device 1 does not show a noticeable change according to the half C of die pad length, whereas the stress at the edge portion E

substantially decreases with an increase in the half C of die pad length. It is thus expected from the level-by-level averages shown in Figs. 9(a) and 9(b) and Figs. 10(a) and 10(b) ~~Figs. 9 and 10~~ that as the die pad section 200 becomes long, i.e., the side 204 of the die pad portion 200 protrudes outside from the side 54 of the semiconductor chip 5, the maximum stress at the edge portion E will be reduced.

Please replace the paragraph beginning on page 20, line 6 with the following amended paragraph:

Fig. 12(a) is a cross-sectional view of a semiconductor device 1 according to a second embodiment of the present invention. The semiconductor device 1 according to the present embodiment is different from the first embodiment in that in a die pad section 200, a through section 207 is defined in a portion where semiconductor chips 4 and 5 overlap each other. The purpose of formation of the through section 207 at the portion where the semiconductor chips 4 and 5 overlap each other is that most of the ~~through section 207 is formed~~ stress is at the portion where the semiconductor chips 4 and 5 overlap each other. ~~Part of~~ However, the through section 207 may be defined in a portion ~~(portion)~~ where [[only]] the semiconductor chip 4 is ~~fixed)~~ not fixed, or in other words at a portion other than the portion where the semiconductor chips 4 and 5 overlap each other, as shown in Fig. 12(b).

Please replace the paragraph beginning on page 21, line 18 with the following amended paragraph:

Figs. 13 shows calculated values of maximum stresses that act on the semiconductor chip 4 where no through section is provided in the die pad section 200 and the through section is defined in the portion in the die pad section 200, where only the semiconductor chip 4 is disposed. When the through section was provided, the maximum stress at a portion above the through section of the semiconductor chip 4 was calculated. When no through section is provided, stress applied to the semiconductor chip 4 at the same position as the position where the through section was provided, was calculated. As is understood from the same drawing, when the through section is provided, the stress concentrates on the portion above the through section of the semiconductor chip 4 and becomes large than that at the time that no through section is provided. At this time, there is a fear that since the strength of one semiconductor chip 4 is provided above the through section, the semiconductor chip 4 is deteriorated at the portion above the through section. Thus, in the present embodiment, major parts of through sections 207 are respectively defined in portions where semiconductor chips 4 and 5 overlap in die pad sections 200 as shown in ~~Fig. 14~~ Figs. 14(a) – 14(d).

Please replace the paragraph beginning on page 22, line 14 with the following amended paragraph:

The through section 207 shown in ~~the same figure (a)~~ Fig. 14(a) has a substantially rectangular central portion 207a and radial portions 207b that extend outwardly from the central portion 207a along diagonal lines. Parts on the leading end sides, of the radial portions 207b are formed at a portion where only the semiconductor chip 4 is disposed, whereas most of the through section 207 is formed at a portion where the semiconductor chips 4 and 5 overlap each other.

Please replace the paragraph beginning on page 22, line 23 with the following amended paragraph:

The through section 207 shown in Fig. 14(b) ~~the same figure (b)~~ has a plurality of bar-shaped portions parallel to one another. Parts of the respective bar-shaped portions are respectively formed at a portion where only the semiconductor chip 4 is disposed, whereas most of the through section 207 is formed at a portion where the semiconductor chips 4 and 5 overlap each other.

Please replace the paragraph beginning on page 23, line 3 with the following amended paragraph:

The through section 207 shown in Fig. 14(c) ~~the same figure (c)~~ has a cross-

shaped portion whose leading ends are at sharp angles. Part of the cross-shaped portion is formed at a portion where only the semiconductor chip 4 is disposed, whereas most of the through portion 207 is formed at a portion where the semiconductor chips 4 and 5 overlap each other.

Please replace the paragraph beginning on page 23, line 10 with the following amended paragraph:

The through section 207 shown in Fig. 14(d) ~~the same figure (d)~~ has a plurality of substantially circular portions. The respective substantially circular portions are formed at a portion where the semiconductor chips 4 and 5 overlap each other.

Please replace the paragraph beginning on page 23, line 15 with the following amended paragraph:

Although the four types of through sections 207 have been shown in the present embodiment, the shapes of the through sections 207 are not limited to these. Most of the through section 207 may be formed at the portion where the semiconductor chips 4 and 5 overlap each other. Incidentally, the semiconductor device 1 according to the present embodiment is manufactured by preparing a lead frame 2 having such through sections 207 as shown in Figs. 14(a)-14(d) ~~Fig. 14~~ and then using a manufacturing method similar to the first embodiment.

Please replace the paragraph beginning on page 27, line 8 with the following amended paragraph:

Incidentally, although the semiconductor chip 5 and the semiconductor chip 500 are shifted to a lead terminal section 220 in the present embodiment, the semiconductor chip 500 may be shifted to a lead terminal section 210. That is, as shown in Fig. 16, the semiconductor chip 400 may be fixed such that the side 403 is located on the side 204 side of the die pad section 200. Further, the semiconductor chip 500 may be fixed to the semiconductor chip 400 in such a manner that in a state in which the surface 502 of the semiconductor chip 500 is placed face to face to the surface 401 of the semiconductor chip [[4]] 400, the side 503 of the semiconductor chip 500 is located inside from the side 403 of the semiconductor chip 400 and the side 504 of the semiconductor chip 500 is located outside from the side 404 of the semiconductor chip 400 and inside from the side 203 of the die pad section 200. Here, the more the length of the side 203 of the die pad section 200, which protrudes outside from the side 404 of the semiconductor chip 400, increases, the more deterioration of the semiconductor chip 500 at an edge portion E can be suppressed due to the reason similar to the first embodiment. A through section 207 is formed at a portion where the semiconductor chips 4, 5, 400 and 500 overlap one another in the die pad section 200.

Please replace the abstract with the following amended abstract:

~~The present invention provides a~~ A semiconductor device ~~which comprises~~ includes a die pad section [[(200)]] having a surface [[(201)]] and a back surface [[(202)]], a first semiconductor chip [[(4)]] having a surface [[(41)]] on which a first electrode section [[(47)]] is formed, and a back surface [[(42)]] fixed to the surface of the die pad section [[(200)]], a second semiconductor chip [[(5)]] having a surface [[(51)]] on which a second electrode section [[(57)]] is formed, and a back surface [[(52)]] fixed to the surface [[(41)]] of the first semiconductor chip [[(4)]], lead terminal sections ~~(210 and 220)~~ respectively electrically connected to the first and second electrode sections ~~(47 and 57)~~, and a resin encapsulating body [[(10)]] that seals the die pad section [[(200)]] and the first and second semiconductor chips ~~(4 and 5)~~. An edge portion [[(54)]] of the second semiconductor chip [[(5)]] protrudes from an edge portion [[(44)]] of the first semiconductor chip [[(4)]]. An edge portion [[(204)]] of the die pad section [[(200)]] protrudes from an edge portion [[(44)]] of the first semiconductor chip [[(4)]].